PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Appellant:	Goruganthu et al.	Examiner:	Souw, B.
Application No.:	09/583,617	Group Art Unit:	2881
Filed:	May 31, 2000	Docket No.:	AMDA.441PA
Title:	Electrical Probing of SOI Circuits		

CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence and the papers, as described hereinabove, are being deposited in the United States Postal Service, as first class mail, in an envelope addressed to: Board of Patent Appeals and Interferences, United States Patent and Trademark Office, P.O. Box 1450, Alexandria, VA 22313-1450, on April 18, 2005.

By: E. M. Nichols
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APPEAL BRIEF

Board of Patent Appeals and Interferences
United States Patent and Trademark Office
P.O. Box 1450
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Customer No. 40581

Sir:

This is an Appeal Brief submitted pursuant to 37 C.F.R. § 41.37 for the above-referenced patent application. Please charge Deposit Account No. 01-0365 (TT3751) in the amount of $500 for this brief in support of appeal as indicated in 37 C.F.R. § 41.20(b)(2). If necessary, authority is given to charge/credit deposit account 01-0365 (TT3751) any additional fees/overages in support of this filing.

I. Real Party in Interest

The real party in interest is the assignee, Advanced Micro Devices.

II. Related Appeals and Interferences

While Appellant is aware of other pending applications owned by the above-identified assignee, Appellant is unaware of any related appeals, interferences or judicial proceedings that would have a bearing on the Board's decision in the instant appeal.

III. Status of Claims

Claims 1, 4-19 and 22-29 are pending and each of the appealed claims is rejected. Claims 2, 3, 20 and 21 have been canceled. The pending claims, as presently amended, may be found in the attached Appendix of Appealed Claims.

IV. Status of Amendments

No amendments were filed subsequent to the final Office Action dated November 16, 2004.

V. Summary of Invention

As set forth in the independent claims involved in the appeal (*i.e.*, claims 1, 16, 17, 24 and 28), an important part of the claimed invention is directed to Appellant's discovery that the insulator layer in an SOI device can be used with a scanning electron beam probe and a circuit-testing device to image a response from the insulator layer (and via the capacitive coupling provided by the insulator layer) in order to analyze the underlying circuitry. *See, e.g.*, page 6, lines 2-4 and page 7, lines 18-21. As discussed below under the heading "Argument," important claimed aspects are directed to such use of electron-beam scanning through the insulator layer and to such use of electron-beam scanning while using the capacitive coupling inherently provided by the insulator layer of an SOI device that is operational.

One example embodiment of the present invention is directed to a method for analyzing a semiconductor die having silicon-on-insulator (SOI) structure and a back side opposite circuitry near a circuit side. *See, e.g.*, Fig. 2, and the discussion at page 6, line 15 – page 9, line 6. The method includes removing substrate from the back side of the

semiconductor die (*e.g.*, 260) and exposing a region of the insulator of the SOI structure where the substrate has been removed (*e.g.*, 270). The method further includes inducing a detectable response from the exposed region as a function of a portion of the circuitry including using an electron beam and detecting secondary electrons generated in response to the electron beam and the portion of the circuitry and, therefrom, analyzing the die. *See, e.g.*, page 7, lines 12-18. Analyzing the die includes using a scanning electron microscope (SEM). *See, e.g.*, page 7, lines 18-20.

Another embodiment of the present invention is directed to a system for analyzing a semiconductor die having SOI structure and a back side opposite circuitry near a circuit side. *See, e.g.*, Fig. 3 and page 9, line 7 – page 11, line 5. The system includes means for removing substrate from the back side of the semiconductor die and exposing a region of the insulator of the SOI structure where the substrate has been removed (such means being, *e.g.*, typically-available substrate removal devices including a focused ion beam, a laser etching device, or an etch chamber having an etch gas used in combination with a mask step) and means for inducing a detectable response from the exposed region as a function of a portion of the circuitry including using an electron beam (such means being, *e.g.*, an electron beam generator, a SEM, or a controller).[1] The system also includes means for detecting the response including detecting secondary electrons generated in response to the electron beam and the portion of the circuitry and, therefrom, analyzing the die wherein analyzing the die includes using a scanning electron microscope (SEM) (such means being, *e.g.*, a detector or a SEM).

Another embodiment of the present invention is directed to a system for analyzing a semiconductor die having SOI structure and a back side opposite circuitry near a circuit side. *See, e.g.*, Fig. 3 and page 9, line 7 – page 11, line 5. The system includes a substrate removal arrangement adapted to remove substrate from the back side of the semiconductor die and expose a region of the insulator of the SOI structure where the portion has been removed. *See, e.g.*, page 6, line 17 – page 7, line 11. The system also includes a probe arrangement adapted to induce a detectable response from the exposed region as a function of

[1] Appellant notes that the two means limitations may optionally be implemented using the same tool. A single structural element may perform two functions and may support two different claim terms. Reed v. Edwards, 26 C.C.P.A. 901, 101 F.2d 550, 554, 40 USPQ 620, 622 (CCPA 1939); *In re Kelley*, 49 C.C.P.A. 1359, 305 F.2d 909, 914, 134 USPQ 397, 401 (CCPA 1962) (as cited in the unpublished decision of *Winbond Elec. Corp. v. Int'l. Trade Comm.*, 4 Fed.Appx. 832, 2001 WL80412 (Fed. Cir. Jan. 13, 2001)).

the circuitry including using an electron beam and including a SEM adapted to provide at least one of: an image of a circuit under analysis and data for probe navigation. *See, e.g.,* page 9, lines 7-17. Also in the system is a detector adapted to detect the response including detecting secondary electrons generated in response to the electron beam and the portion of the circuitry and, therefrom, analyze the die. *See, e.g.,* page 9, line 12 – page 10, line 12.

Another embodiment of the present invention is directed to a method for analyzing a die having SOI structure and a back side opposite circuitry near a circuit side. *See, e.g.*, Fig. 2, and the discussion at page 6, line 15 – page 9, line 6. The method includes removing substrate from the back side of the semiconductor die and exposing a region of the insulator of the SOI structure where the substrate has been removed (*e.g.*, 270) and inputting electrical signals to the die to operate the die in a continuous loop known to cause a failure in a portion of the circuitry in the die. *See, e.g.,* page 10, lines 13-20. The method also includes directing an electron beam to the exposed region of the insulator and inducing a detectable response therefrom as a function of the portion of the circuitry failing. The die is then analyzed. *See, e.g.*, page 7, lines 12-20 and page 10, lines 19-20.

Another embodiment of the present invention is directed to a method for detecting logic states of a plurality of circuit nodes in a die having SOI structure and a back side opposite circuitry near a circuit side. *See, e.g.*, Fig. 2, and the discussion at page 6, lines 5-6 and line 15 – page 9, line 6. The method includes removing substrate from the back side of the semiconductor die and exposing a region of the insulator of the SOI structure where the substrate has been removed and adjacent to the plurality of circuit nodes (*e.g.*, 270). The method also includes inputting electrical signals to the die to cause the plurality of circuit nodes to take on logical states and scanning an electron beam across the exposed region of the insulator and inducing a detectable response therefrom as a function of the logic states of the circuit nodes adjacent to the exposed region upon which the electron beam is directed. The die is then analyzed. *See, e.g.,* page 7, line 12 – page 8, line 21.

As required by 37 C.F.R. § 41.37(c)(1)(v), a concise explanation of the subject matter defined in the independent claims involved in the appeal is provided herein. Appellant notes that representative subject matter is identified for these claims; however, the abundance of supporting subject matter in the application prohibits identifying all textual and diagrammatic references to each claimed recitation. Appellant thus submits that other application subject

matter, which supports the claims but is not specifically identified above, may be found elsewhere in the application. Appellant further notes that this summary does not provide an exhaustive or exclusive view of the present subject matter, and Appellant refers to the appended claims and their legal equivalents for a complete statement of the invention.

VI. Grounds of Rejection

A. Claims 1, 4-12, 16-19, 21 and 23 are rejected under 35 U.S.C. § 103(a) over Yoshida (U.S. Patent No. 6,137,295) in view of Talbot *et al.* (U.S. Patent No. 6,091,249) or Steffan *et al.* (U.S. Patent No. 6,200,823).

B. Claims 13 and 24 are rejected under 35 U.S.C. § 103(a) over Yoshida in view of Talbot *et al.* or Steffan *et al.* and further in view of Zingher (U.S. Patent No. 4,443,278), Gauthier *et al.* (U.S. Patent No. 4,172,228), and Nakasuji (U.S. Patent No. 6,465,783).

C. Claim 14 is rejected under 35 U.S.C. § 103(a) over Yoshida in view of Talbot *et al.* or Steffan *et al.* and further in view of Ishihara *et al.* (U.S. Patent No. 6,185,324).

D. Claim 15 is rejected under 35 U.S.C. § 103(a) over Yoshida in view of Talbot *et al.* or Steffan *et al.* and further in view of Lo *et al.* (U.S. Patent No. 6,344,750) and Cole, Jr. (U.S. Patent No. 5,523,694).

E. Claim 22 is rejected under 35 U.S.C. § 103(a) over Yoshida in view of Talbot *et al.* or Steffan *et al.* and further in view of Kim *et al.* (U.S. Patent No. #2002/0043628A1) and Yamazuki *et al.* (U.S. Patent No. 6,038,018).

F. Claims 24-27 are rejected under 35 U.S.C. § 103(a) over Yoshida in view of Nakasuji, Gauthier *et al.*, Zingher, and Ishihara *et al.*

G. Claims 28 and 29 are rejected under 35 U.S.C. § 103(a) over Yoshida in view of Lo et al. (U.S. Patent No. 6,504,393).

H. Claims 28 and 29 are rejected under 35 U.S.C. § 103(a) over Yoshida in view of unidentified prior art and unintelligible rationale.

VII. Argument

The rejections of claims 1, 4-19, 22 and 23 (A-E), rely on an improper modification of the first embodiment of the primary '295 reference. The Examiner's proposed modification of the '295 reference to replace the '295 electron beam with a SEM directly opposes the '295 teachings thereby undermining and destroying both the purpose and operation of the '295 teachings – which is in direct contradiction of 35 U.S.C. § 103(a) and MPEP § 2143.01 (the asserted combination cannot either undermine or destroy the purpose/operation of the primary reference).

The purpose of the '295 reference is defined in its background, summary and claims, and detailed description. In its background, the '295 reference teaches that prior art testing approaches are limited because based merely on observation, large scale integrated circuits cannot be analyzed adequately. *See* column 2, lines 16-23.

In its summary and claims, the '295 reference defines the operation and purpose as operating the device while irradiating an electron beam *at a particular diffusion region* in the device (column 2, lines 32-38). Thus, the '295 reference teaches this approach as involving the pin-pointing of the particular region in the device, or "observing," by "designating a position to be observed according to the layout diagram" (column 2, lines 61-62), and/or "matching a needle of a probe card with a predetermined position of a wafer by magnifying means" (column 2, lines 67 - column 3, line 3). The claims of the '295 reference are directed to observation *at a particular diffusion region* in the device (claim 1), with most of the dependent claims specifically requiring "matching a needle of a probe card with a predetermined position of" for observation *at the particular diffusion region.*

In its detailed description, the '295 reference reiterates this point by way of its discussion at column 6, lines 1-45, and by way of its ultimate statement at column 6, lines 33-34: "To detect a defect, it is necessary to designate a location to be observed." Appellant notes that the '295 reference's discussion of this *necessary* location designation is with respect to the same first embodiment relied upon by the Examiner maintaining the rejections.

In view of the above, it can be appreciated that the Examiner's proposal to insert a SEM into the '295 reference's first embodiment would eliminate this focus-point testing of the '295 reference. Instead of first taking the "necessary [step] to designate a location to be observed," the Examiner's proposal would simply scan a beam across a circuit instead of

focusing on a predetermined location where a probe is set to contact the circuit for isolating the operation per the signals driving the circuit via the circuit tester. This general scanning will fail to identify the defects sought after by the '295 teachings as it does not teach any way to assimilate data between that which is observed generally and that which the circuit tester would be exercising. Since the proposed modification is inconsistent with the purpose and operation of the '295 reference, the proposed combination fails to support any suggestion or motivation to combine the references. Without a presentation of the requisite evidence of motivation, each of these Section 103(a) rejections is improper and Appellant accordingly requests that the rejections be reversed.

With respect to the secondary reference (U.S. Patent 6,200,283 to Steffan *et al.*) as used in all of the above rejections, each of these rejections in view of this '283 reference is improper because the '283 reference is not "prior art" pursuant to 35 U.S.C. § 103(c). As set forth in MPEP § 706.02(l)(1), effective November 29, 1999, subject matter which was prior art under former 35 U.S.C. § 103 via 35 U.S.C. § 102(e) is now disqualified as prior art against the claimed invention if that subject matter and the claimed invention "were, at the time the invention was made, owned by the same person or subject to an obligation of assignment to the same person." The amendment to 35 U.S.C. § 103(c) applies to all utility, design and plant patent applications filed on or after November 29, 1999.

In view of the above, Appellant submits that U.S. Patent Number 6,200,283 is, and has been over the entire relevant time period when the instant invention was made, owned by the same entity, Advanced Micro Devices ("AMD"), or subject to an obligation of assignment to the same entity as is the instant application. These common assignments are evidenced by the instant assignment recorded at reel/frame number 010855/0047 and the cover page of U.S. Patent Number 6,200,283. Thus, the '283 patent is not prior art with respect to the instant invention and the rejections should be reversed.

Accordingly, Appellant submits that each of the rejections of claims 1, 4-19, 22 and 23 is improper because the Examiner's proposed modification of the '295 reference undermines and/or destroys the purpose and operation of the '295 teachings; and each of the combinations relying on the '283 reference fails to present rationale based upon "prior art" teachings. Thus, Appellant requests that each of the rejections of claims 1, 4-19, 22 and 23 be reversed.

Regarding claims 1, 4-12, 16-19, 21 and 23 (Ground A above), the rejection is improper because the Examiner fails to present evidence of motivation to combine the references as asserted and attempts to present new grounds of rejection by changing the asserted manner of combination.

The Examiner fails to present any evidence from the cited references in support of the asserted combination. The MPEP states that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either explicitly or implicitly in the references themselves or in the knowledge generally available to one of ordinary skill in the art. MPEP § 2143.01. The Examiner acknowledges at page 3, that the '295 reference fails to recite the use of a scanning electron microscope to analyze the die. To overcome this deficiency, the Examiner merely alleges that a SEM "is a versatile apparatus that can be used for a variety of other purposes with high accuracies and a lot of device sophistication . . . as compared to the EB tester used by Yoshida ['295 reference], which is usually much simpler and very specific in design and structure, while being limited in the variety of tasks it is capable to execute" without citing any teachings in support of such proposed modification. Without the requisite presentation of evidence of motivation, the Section 103(a) rejection is improper. Accordingly, Appellant respectfully traverses the rejection and requests that it be reversed.

Moreover, the Examiner acknowledges the deficiency of the rejection presented in the first Office Action dated May 24, 2004, by changing the asserted combination of references in the final Office Action dated November 16, 2004. The Examiner's rationale in the first Office Action proposed using "an SEM as taught by Talbot et al. and/or Steffan et al. in place of Yoshida's EB tester." In the following, final Office Action, the Examiner instead proposes using "the electron beam part of an SEM to replace Yoshida's EB." Appellant submits that this rationale change constitutes new grounds of rejection and therefore, the finality of the November 16th Office Action is improper. Appellant accordingly requests that the rejection be reversed.

Regarding claims 13 and 24 (Ground B above), the rejection is improper because the Examiner fails to present a combination of references that corresponds to the claimed invention.

Appellant notes that contrary to the assertion at page 7, claim 24 is independent, thus claim 12 is not a parent claim to claim 24 and any rationale presented with respect to claim 12 is irrelevant as to the limitations of claim 24. Moreover, the Examiner acknowledges at page 11 that the combination of references asserted against claim 13 fails to teach each of the limitations of claim 24 and by further requiring the teachings of the '324 reference. Thus, the Section 103(a) rejection of claim 24 is improper and should be reversed.

With respect to claim 13, the Examiner fails to assert that the combination of references teaches "inputting signals known to induce a failure in the die." Without an assertion of correspondence, the Section 103(a) rejection is improper and should be reversed.

Regarding dependent claim 14 (Ground C above), the rejection is improper because the Examiner fails to present any evidence of motivation from the cited references to modify the primary '295 reference, as asserted.

The rejection of dependent claim 14 is improper for the reasons discussed above in connection with independent claim 1. The rejection of claim 14 relies upon the same primary combination of the '295 reference with the '249 or '823 reference that is shown to be insufficient grounds of rejection as discussed above. "If an independent claim is nonobvious under 35 U.S.C. § 103, then any claim depending therefrom is nonobvious." MPEP § 2143.03; *citing In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988). Moreover, the Examiner attempts to overcome this deficient combination by erroneously asserting that the claimed limitations directed to inputting signals in a continuous loop are an automation of a conventional method that "has been normally implemented manually." This is untrue. The speed at which the claimed intricate semiconductor circuitry operates renders a manual input of signals impractical. The circuitry is operated with a continuous loop in order to monitor the changing response of the die. The Examiner later admits at page 8 that this process is not implemented manually and further fails to present any evidence from the cited references in support of the proposed modification. Thus, the rejection of dependent claim 14 under 35 U.S.C. § 103 should be reversed.

Regarding dependent claim 15 (Ground D above), the rejection is improper because the Examiner fails to present any evidence of motivation from the cited references to modify the primary '295 reference, as asserted.

The rejection of dependent claim 15 is improper for the reasons discussed above in connection with independent claim 1. The rejection of claim 15 relies upon the same primary combination of the '295 reference with the '249 or '823 reference that is shown to be insufficient grounds of rejection as discussed above. "If an independent claim is nonobvious under 35 U.S.C. §103, then any claim depending therefrom is nonobvious." MPEP § 2143.03; *citing In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988). Moreover, the Examiner fails to present evidence of why the skilled artisan would modify the '295 reference, as asserted. The '295 reference plainly teaches various methods for detecting defects without using a non-defective die; indeed, these various methods are recited as specific "objects" of the invention. *See, e.g.,* column 3, lines 38-55. For example, the '295 reference teaches away from such a comparison because it positively identifies the location and uses specific test signals as recited in column 6, lines 33-34, indicating that "it is necessary to designate a location to be observed." Therefore, one of skill in the art would not be motivated to modify the '295 reference to include limitations directed to a comparison to a reference die and the Examiner has not presented any evidence from the cited references in support of the proposed modification. Thus, the rejection of dependent claim 15 under 35 U.S.C. § 103 should be reversed.

Regarding dependent claim 22 (Ground E above), the rejection is improper because the Examiner fails to present any evidence of motivation from the cited references to modify the primary '295 reference, as asserted.

The rejection of dependent claim 22 is improper for the reasons discussed above in connection with independents claim 1 and 17. The rejection of claim 22 relies upon the same primary combination of the '295 reference with the '249 or '823 reference that is shown to be insufficient grounds of rejection as discussed above. "If an independent claim is nonobvious under 35 U.S.C. §103, then any claim depending therefrom is nonobvious." MPEP § 2143.03; *citing In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988). Thus, the rejection of dependent claim 22 under 35 U.S.C. § 103 should be reversed.

Regarding claims 24-27 (Ground F above), the rejection is improper because the Examiner fails to assert correspondence to each of the claimed limitations.

The Examiner fails to assert that the cited combination of references teaches directing an electron beam to the exposed region of the insulator, as claimed. Without any assertion of correspondence the rejection is improper. Appellant accordingly requests that the rejection be reversed.

Regarding claims 28-29 (Ground G above), the rejection is improper because the Examiner fails to assert correspondence to each of the claimed limitations.

The Examiner fails to assert that the cited combination of references corresponds to each of the claimed limitations because the Examiner ignores limitations in claims 28 and 29 directed to scanning an electron beam across the exposed region. Without any assertion of correspondence the rejection is improper. Appellant accordingly requests that the rejection be reversed.

Regarding the rejection of claims 28 and 29 under 35 U.S.C. § 103(a) over Yoshida in view unidentified prior art, the Examiner fails to present a coherent rejection.

This rejection, as set forth at page 12, lines 9-14, is unintelligible. The prior art relied upon for this rejection is ambiguous, and the rationale refers to claims 26 and 27 which are unrelated to claims 28 and 29. While this rejection likely includes inadvertent misstatements, Appellant has unsuccessfully attempted to decipher the intent behind this rejection. For example, the most likely interpretation is that the Examiner intended to refer to claims 26-27 at line 9 rather than 28-29; however, this assumption is illogical because the rational provided refers to a claim that includes "logical states" and such a claim term is not present in either claim 26 or claim 27. Appellant submits that this rejection is without reason and therefore, fails to present both a *prima facie* case and any argument that would comply with 35 U.S.C. § 132. Accordingly, Appellant requests that this rejection be reversed.

VIII. Conclusion

In view of the above, Appellant submits that the rejections are improper, the claimed invention is patentable, and that the rejections of claims 1, 4-19 and 22-29 should be reversed. Appellant respectfully requests reversal of the rejections as applied to the appealed claims and allowance of the entire application.

Authority to charge the undersigned's deposit account was provided on the first page of this brief.

Respectfully submitted,

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APPENDIX OF APPEALED CLAIMS

1. A method for analyzing a semiconductor die having silicon-on-insulator (SOI) structure and a back side opposite circuitry near a circuit side, the method comprising:

removing substrate from the back side of the semiconductor die and exposing a region of the insulator of the SOI structure where the substrate has been removed; and

inducing a detectable response from the exposed region as a function of a portion of the circuitry including using an electron beam and detecting secondary electrons generated in response to the electron beam and the portion of the circuitry and, therefrom, analyzing the die wherein analyzing the die includes using a scanning electron microscope (SEM).

4. The method of claim 1, wherein analyzing the die includes detecting a first magnitude of secondary electrons from a selected circuit portion and a second magnitude of secondary electrons detected from another circuit portion, the first and second magnitudes of secondary electrons being indicative of an electric characteristic differential between the selected circuit portion and the other circuit portion.

5. The method of claim 4, further comprising detecting secondary electrons from a plurality of circuit portions and obtaining an image of the die that represents variations in voltage across the plurality of circuit portions.

6. The method of claim 1, wherein using the electron beam includes pulsing the beam, and wherein analyzing the die includes obtaining a waveform response to the pulsed beam.

7. The method of claim 6, further comprising coupling a power supply to the die and inputting electrical signals to the die to generate a response.

8. The method of claim 1, wherein inducing a detectable response includes inducing a response as a function of an electrical characteristic of a source/drain region in the die.

9. The method of claim 1, wherein inducing a detectable response includes using a buried oxide (BOX) portion of the SOI structure as a dielectric.

10. The method of claim 9, wherein removing a portion of substrate from the back side of the semiconductor die includes exposing a portion of the BOX.

11. The method of claim 1, wherein analyzing the die includes post-manufacturing analysis.

12. The method of claim 11, wherein analyzing the die includes obtaining a response for electrical stimulus applied to circuitry in the die.

13. The method of claim 12, wherein inputting electrical signals includes inputting signals known to induce a failure in the die.

14. The method of claim 12, wherein inputting electrical signals includes inputting signals in a continuous loop.

15. The method of claim 1, further comprising inducing a detectable response from a non-defective die in the same manner as the die being analyzed, the non-defective die having the same design as the die being analyzed, and comparing the analysis of the dies.

16. A system for analyzing a semiconductor die having silicon-on-insulator (SOI) structure and a back side opposite circuitry near a circuit side, the system comprising:

means for removing substrate from the back side of the semiconductor die and exposing a region of the insulator of the SOI structure where the substrate has been removed;

means for inducing a detectable response from the exposed region as a function of a portion of the circuitry including using an electron beam; and

means for detecting the response including detecting secondary electrons generated in response to the electron beam and the portion of the circuitry and, therefrom, analyzing the die wherein analyzing the die includes using a scanning electron microscope (SEM).

17. A system for analyzing a semiconductor die having silicon-on-insulator (SOI) structure and a back side opposite circuitry near a circuit side, the system comprising:

a substrate removal arrangement adapted to remove substrate from the back side of the semiconductor die and expose a region of the insulator of the SOI structure where the portion has been removed;

a probe arrangement adapted to induce a detectable response from the exposed region as a function of a portion of the circuitry including using an electron beam and including a SEM adapted to provide at least one of: an image of a circuit under analysis and data for probe navigation; and

a detector adapted to detect the response including detecting secondary electrons generated in response to the electron beam and the portion of the circuitry and, therefrom, analyze the die.

18. The system of claim 17, further comprising a controller adapted to control the substrate removal arrangement.

19. The system of claim 18, wherein the controller is adapted to control the substrate removal arrangement to remove sufficient substrate to facilitate the inducing of a response from the exposed region as a function of a portion of the circuitry.

22. The system of claim 17, wherein the SEM also includes the detector and is further adapted to obtain an image of the die having light and dark areas, the dark areas being indicative of circuit portions having a positive voltage greater than that of lighter areas.

23. The system of claim 17, further comprising a tester adapted to introduce electrical stimulus to the die.

24. A method for analyzing a die having silicon-on-insulator (SOI) structure and a back side opposite circuitry near a circuit side, the method comprising:

removing substrate from the back side of the semiconductor die and exposing a region of the insulator of the SOI structure where the substrate has been removed;

inputting electrical signals to the die to operate the die in a continuous loop known to cause a failure in a portion of circuitry in the die; and

directing an electron beam to the exposed region of the insulator and inducing a detectable response therefrom as a function of the portion of the circuitry failing and, therefrom, analyzing the die.

25. The method of claim 24, wherein inducing a detectable response therefrom as a function of the portion of the circuitry failing includes detecting a change in secondary electrons emitted from the exposed region of the insulator.

26. The method of claim 24, wherein directing an electron beam to the exposed region of the insulator and inducing a detectable response therefrom as a function of the portion of the circuitry failing comprises detecting a failure of the die in response to detecting an uninhibited emission of secondary electrons.

27. The method of claim 24, wherein directing an electron beam to the exposed region of the insulator and inducing a detectable response therefrom as a function of the portion of the circuitry failing comprises detecting a failure of the die in response to detecting an inhibited emission of secondary electrons.

28. A method for detecting logic states of a plurality of circuit nodes in a die having silicon-on-insulator (SOI) structure and a back side opposite circuitry near a circuit side, the method comprising:

removing substrate from the back side of the semiconductor die and exposing a region of the insulator of the SOI structure where the substrate has been removed and adjacent to the plurality of circuit nodes;

inputting electrical signals to the die to cause the plurality of circuit nodes to take on logical states; and

scanning an electron beam across the exposed region of the insulator and inducing a detectable response therefrom as a function of the logic states of the circuit nodes adjacent to the exposed region upon which the electron beam is directed and, therefrom, detecting the logic states of the plurality of circuit nodes.

29. The method of claim 28, wherein scanning an electron beam across the exposed region of the insulator and inducing a detectable response therefrom as a function of the logic states of the circuit nodes comprises:

detecting a non-positive logical state at one of the plurality of circuit nodes as a function of detecting an uninhibited emission of secondary electrons; and

detecting a positive logical state at one of the plurality of circuit nodes as a function of an inhibited emission of secondary electrons.

EVIDENCE APPENDIX

None.

RELATED PROCEEDINGS APPENDIX

None.